

A Flexible Amorphous Silicon Photovoltaic Module for Portable Electronics

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Abstract — This paper reports on a monolithic 10 cm × 10 cm area PV module integrating an array of 72 a-Si:H n-i-p cells on a thin polyethylene-naphtalate substrate. The design optimization and device performance analysis are performed using a two-dimensional distributed circuit model of the photovoltaic cell. Experimental results show that the shunt leakage is one of the factors reducing the device performance. Using the LBIC technique, the multiple micro-shunts in the n-i-p cell were detected. The mechanism of electrical shunts formation is proposed and discussed.

Keywords: solar cells, thin films, amorphous silicon.

I. INTRODUCTION

Flexible hydrogenated amorphous silicon (a-Si:H) solar cells on thin plastic substrates are of great interest for a wide variety of engineering applications. Flexible devices can be rolled for transportation, installed on curved surfaces, and they are less likely to be damaged by mechanical friction and vibrations. These advantages make possible for portable electronic devices to cover part of their power demand from solar energy.

Regardless of the intense research efforts directed to the development of flexible a-Si:H solar cells on low-cost plastic substrates, these devices still exhibit considerably lower performance in comparison to that for glass-based equivalents. The major technological challenge is deposition of doped- and undoped a-Si:H layers with required electronic properties at temperatures lower than that for solar cells on glasses or metal foils [1]. The increased shunt leakage in a-Si:H cells on the plastic substrate is another challenging issue [2]. In this contribution, we report on a monolithic a-Si:H-based photovoltaic module utilizing the 100 μm thick polyethylene-naphtalate (PEN) substrate. The nature of observed micro-shunts in the p-i-n cells is under discussion.

II. DEVICE DESIGN, FABRICATION AND MODELLING

Figure 1 shows a photograph of the developed PV module and cross-sectional view of two cells connected in series. The module of 10 cm × 10 cm area consists of 72 rectangular cells on the PEN substrate. The individual cells are connected in series forming eight rows with connection pads. The novelty in the device design is in the backside encapsulation and front buffer silicon-oxynitride layers incorporated for

device integrity. The a-Si:H n-i-p cell integrates Al/Cr and ZnO:Al as back and top electrodes, respectively. Two 0.3 mm wide Al fingers are symmetrically placed on the ZnO:Al electrode to reduce the emitter resistance. The photosensitive area is 1 × 0.8 cm².

In the developed fabrication process, three shadow masks are used in sputtering steps to form the bottom and top electrodes, and top metallization. The first step is sputtering of Al/Cr layers through mask #1. Here, Cr serves as an adhesion layer providing a low contact resistance at the metal/n-layer interface. Then, the n-i-p stack is deposited using a 13.56 MHz PECVD system at 150 °C substrate temperature. The deposition conditions are reported elsewhere [3]. The formation of ZnO:Al top electrodes is performed by sputtering through shadow mask #2 at 140 °C substrate temperature. To perform via opening, the n-i-p stack is selectively etched through shadow mask #3 in the reactive ion etching (RIE) system. Finally, the Al fingers and contact pads are sputtered through shadow mask #3.

The design optimization and device performance analysis are performed using a two-dimensional distributed circuit model of the photovoltaic cell. The circuit simulator SPICE is used to calculate current and potential distributions in a network of sub-cell circuits, and also to map Joule losses in the front TCO electrode and the metal grid (Fig. 2).

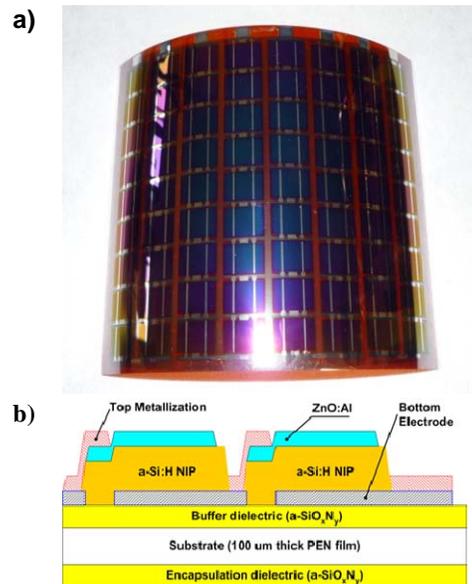


Fig. 1. (a) Photograph of the PV module, and (b) cross-sectional view of two cells connected in series.

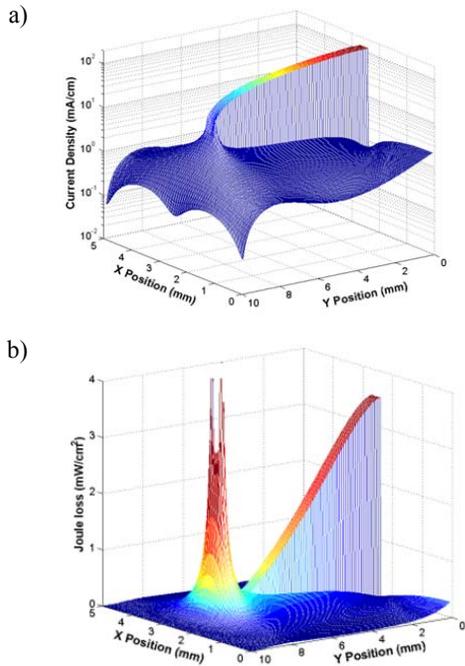


Fig. 2. (a) Current density distribution, and (b) Joule losses in the TCO electrode and metal finger under AM1.5 illumination conditions.

III. DEVICE CHARACTERIZATION

Device characterization shows that the open circuit voltage and fill factor are lower than the calculated values due to existence of resistive shunts in some cells in the module. Current-voltage characteristics of all individual a-Si:H p-i-n cells in the module were measured and analyzed to better understand the issue. It is concluded that the shunt current varies linearly with biasing voltage, what can be represented as a shunt resistance (R_{sh}). The shunt resistance varies in wide range from 10 to $10^5 \Omega$.

The performed laser beam induced current (LBIC) experiments show the presence of multiple shunts. The *ac* component of the output voltage was measured when the device impedance was low ($< 1 \text{ k}\Omega$). Figure 3 shows a LBIC signal map indicating the shunt position manifested as decreased LBIC signal. In the absence of shunts the signal is constant over the whole area, excluding the metal finger area due to light blockage. Using the developed SPICE model, the LBIC signal was also simulated considering a single shunt at different locations. Modelling shows that the shunting microdefect affects the LBIC signal from an area much larger than its actual size since current from the surrounding area is shunted through the defect. The magnitude of signal variation depends on the sheet resistance of the TCO layer. This is in good agreement with the experimental LBIC results.

To understand the nature of electrical shunts, we analyzed the change in the surface roughness of all layers comprising

individual solar cells throughout fabrication process. AFM surface scan of the a-Si:H layer has revealed random surface peaks with height up to 150 nm. The density of these defects is much higher than what is expected from external contamination. Multiple experiments have confirmed that the defects appear after deposition of dielectric or semiconductor layers, or even after sputtering of metal layers on the PEN substrate. The reason is that cyclic oligomers, which are present in PEN, can migrate to the surface forming crystals, if the film is held at temperatures $> 100^\circ\text{C}$ for tens of minutes. The observed substrate defects may form microscopic pinholes, which are filled with highly conductive top layer material at the final process step, resulting in ohmic shunts.

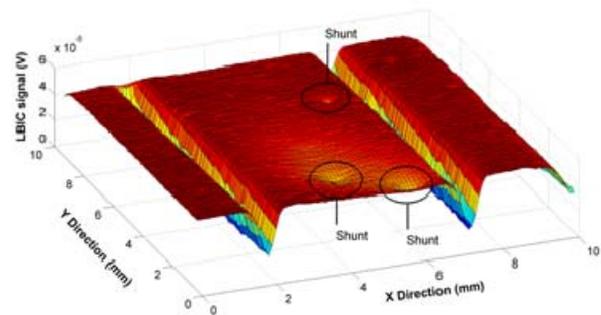


Fig. 3. LBIC signal for cell with multiple shunts.

IV. CONCLUSION

This study shows that the shunt leakage is a major factor reducing the performance of a Si:H solar cells on PEN plastic films. The presence of multiple ohmic micro-shunts is confirmed by the LBIC technique. The formation of micro-shunts is attributed to surface defects in plastic foils, which are thermally induced during the device fabrication.

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